

STM32MP13XXAF_LPDDR3

Schematics not complete, only for layout example

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STM32MP13XXAF_LPDDR3_TOP.SchDoc



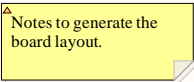
Note

Legend

General comment such as function title, configuration, ...

Text to be added to silkscreen.

Warning text.



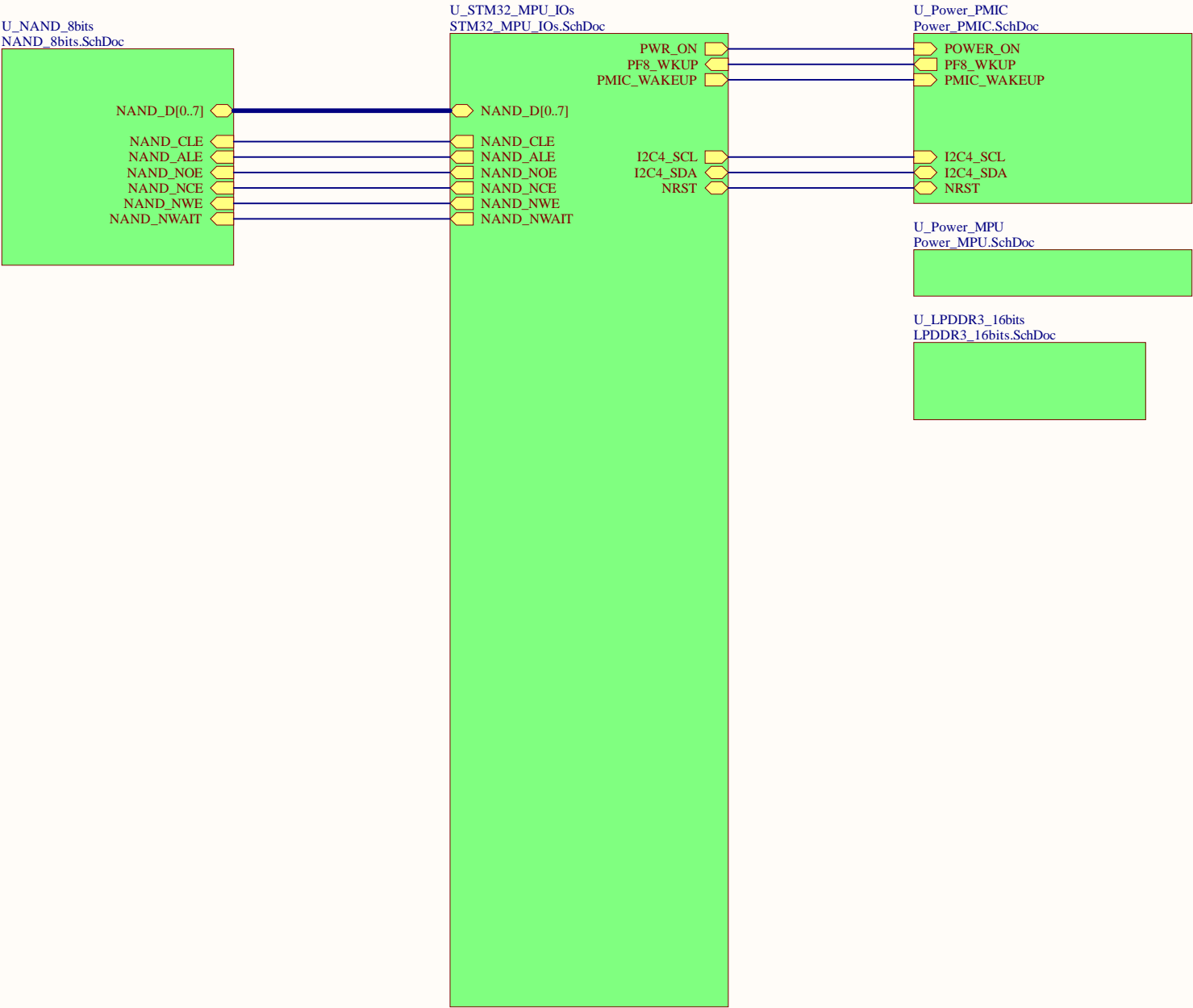
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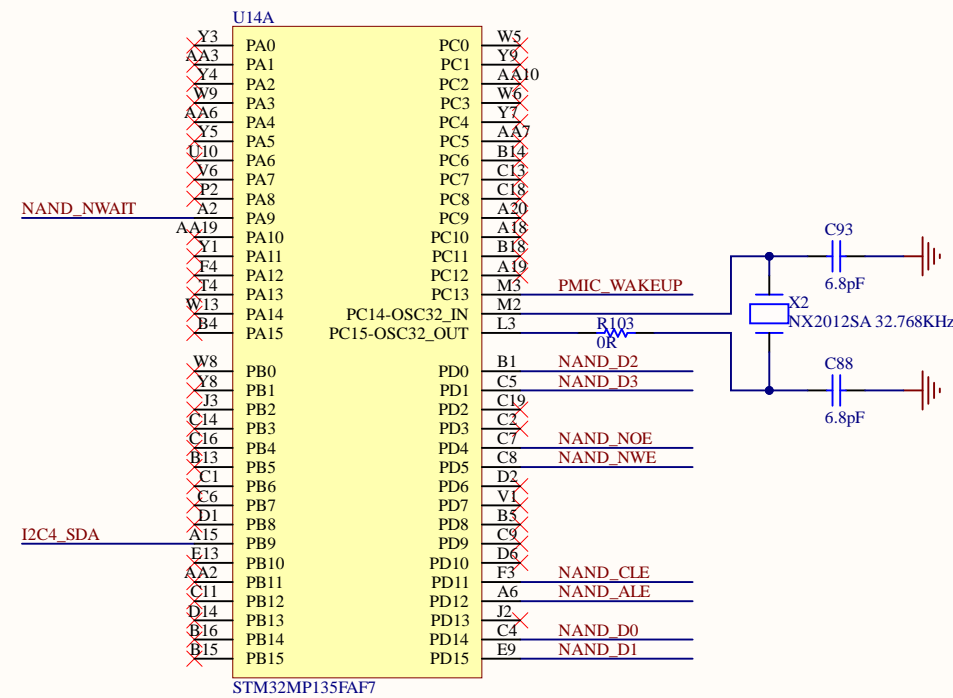
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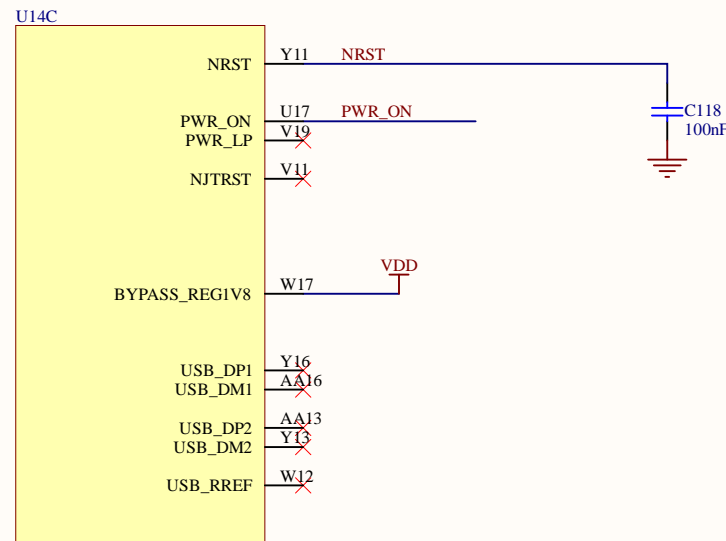
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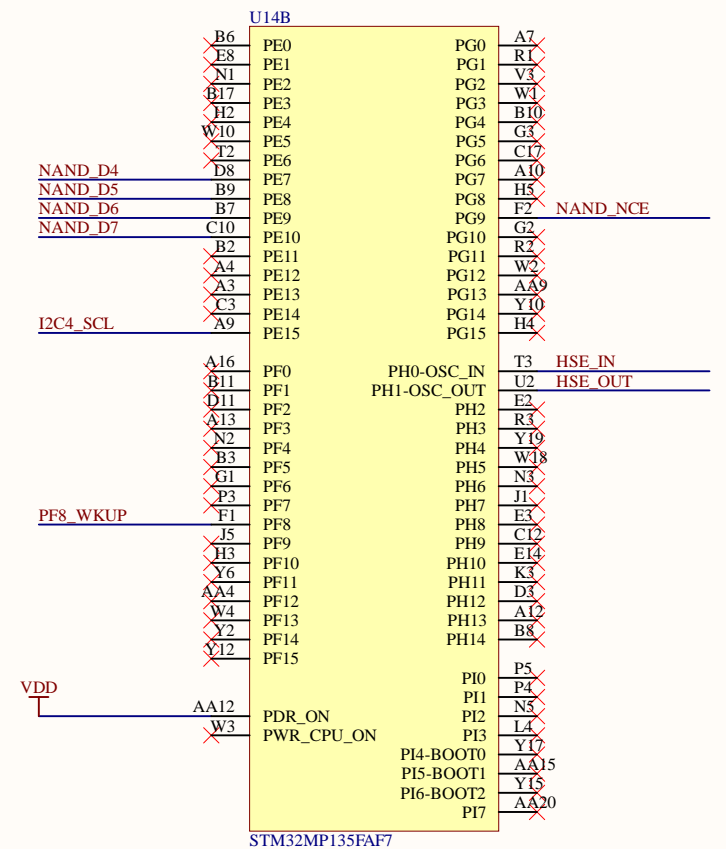




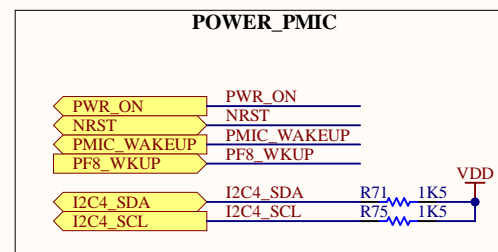
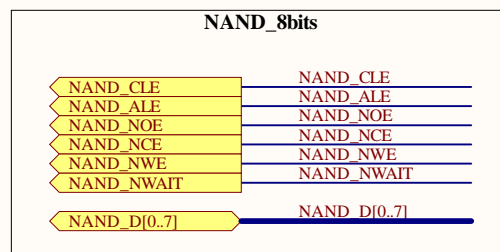
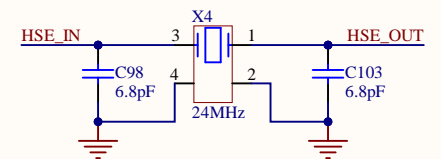
STM32MP135FAF7

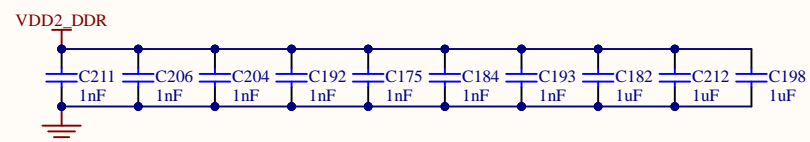


STM32MP135FAF7



STM32MP135FAF7





The schematic diagram illustrates the power supply network for the STM32MP135FA7. It shows the following components and connections:

- Power Pins and Connections:**
 - VDD:** Connected to VDDA1V1_REG, VDDA1V8_REG, VDDSD1, VDDSD2, VDD_PLL, VDD_PLL2, VDD_ANA, VDDA, VREF+, VREF-, VBAT, and VDD3V3_USBHS.
 - VDDA1V1_REG:** Connected to VDD.
 - VDDA1V8_REG:** Connected to VDD.
 - VDDSD1:** Connected to VDD.
 - VDDSD2:** Connected to VDD.
 - VDD_PLL:** Connected to VDD.
 - VDD_PLL2:** Connected to VDD.
 - VDD_ANA:** Connected to VDD.
 - VDDA:** Connected to VDD.
 - VREF+:** Connected to VDD.
 - VREF-:** Connected to VDD.
 - VBAT:** Connected to VDD.
 - VDD3V3_USBHS:** Connected to VDD.
- Capacitors:**
 - C216 (2.2uF):** Connected to VDD and ground.
 - C217 (2.2uF):** Connected to VDD and ground.
 - C171 (1uF):** Connected to VDD and ground.
 - C173 (1uF):** Connected to VDD and ground.
 - C214 (1uF):** Connected to VDD and ground.
 - C219 (1uF):** Connected to VDD and ground.
 - C220 (100nF):** Connected to VDD and ground.
 - C192 (100nF):** Connected to VDD and ground.
 - C119 (100nF):** Connected to VDD and ground.
- Resistors:**
 - R133 (0R):** Connected to VDD and ground.
 - R192 (0R):** Connected to VDD and ground.
- Inductors:**
 - L2:** Connected to VDD and ground.

The diagram is labeled "STM32MP135FA7".

VDD_CORE	G11	VDD_CORE	VSS	A1
	J11	VDD_CORE	VSS	A21
	J15	VDD_CORE	VSS	B12
	L7	VDD_CORE	VSS	D16
	L9	VDD_CORE	VSS	E5
	L13	VDD_CORE	VSS	E6
	N10	VDD_CORE	VSS	E11
	N13	VDD_CORE	VSS	E16
	N15	VDD_CORE	VSS	F5
	R10	VDD_CORE	VSS	F17
	R13	VDD_CORE	VSS	F18
	U12	VDD_CORE	VSS	F21
	U14	VDD_CORE	VSS	G8
		VDD_CORE	VSS	G12
VDD_CPU	E7	VDD_CPU	VSS	G14
	E10	VDD_CPU	VSS	H7
	G5	VDD_CPU	VSS	H15
	G7	VDD_CPU	VSS	J10
	G10	VDD_CPU	VSS	J12
	K5	VDD_CPU	VSS	K9
	K7	VDD_CPU	VSS	K10
VDD	E12	VDD	VSS	K11
	G9	VDD	VSS	K12
	G13	VDD	VSS	K13
	J7	VDD	VSS	K21
	J9	VDD	VSS	L5
	J13	VDD	VSS	L10
	M5	VDD	VSS	L12
	N7	VDD	VSS	L15
	N9	VDD	VSS	L17
	N12	VDD	VSS	M1
	R5	VDD	VSS	M7
	R7	VDD	VSS	M9
	R9	VDD	VSS	M10
	R12	VDD	VSS	M11
	U7	VDD	VSS	M12
	W11	VDD	VSS	M13
VDD2_DDR	E15	VDDQ_DDR	VSS	N11
	G15	VDDQ_DDR	VSS	P7
	G17	VDDQ_DDR	VSS	P15
	K15	VDDQ_DDR	VSS	R8
	K17	VDDQ_DDR	VSS	R11
	M15	VDDQ_DDR	VSS	R14
	M17	VDDQ_DDR	VSS	T1
	R15	VDDQ_DDR	VSS	T5
	R17	VDDQ_DDR	VSS	T17
	U15	VDDQ_DDR	VSS	T21
		VDDQ_DDR	VSS	U5
			VSS	U6
			VSS	U11
			VSS	U13
			VSS	U16
C217 2.2uF	V14	VDDA1V1_REG	VSS	V16
	W15	VDDA1V8_REG	VSS	W16
			VSS	AA1
			VSS	AA21
	E17	VDDSD1		
	C15	VDDSD2		
VDD	K2	VDD_PLL	VSS_PLL	K1
	Y18	VDD_PLL2	VSS_PLL2	AA18
	V2	VDD_ANA	VSS_ANA	U3
	U8	VDDA	VSSA	U9
	W7	VREF+	VSS_USBHS	Y14
	V8	VREF-		
	L2	VBAT		
VDD_USB	W14	VDD3V3_USBHS		
C119				

